UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/539,926	06/14/2005	Sadamu Ishidu	20239/0202616-US0	8405

7278 7590 04/06/2006

DARBY & DARBY P.C.
P. O. BOX 5257
NEW YORK, NY 10150-5257

EXAMINER	
CRANE, SARA W	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 04/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

H/A

Office Action Summary	Application No.	Applicant(s)	
	10/539,926	ISHIDU ET AL.	
	Examiner	Art Unit	
	Sara W. Crane	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-3 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-3 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Japan 11-026647 in view of Tamaoki et al. and Yamamoto et al.

With respect to claim 1, the Japanese reference 11-026647 shows a light emitting semiconductor element 34, mounted on a substrate 1 (see figure 1). The distance corresponding to H would be the distance from the top of the substrate (where the semiconductor is mounted) to the bottom of the substrate. It is clear from figure 1 that this distance is two or three times either length dimension of the semiconductor element, certainly much greater than 0.3 times the length dimension of the semiconductor element. Tamaoki et al. teaches that a typical light emitting area of a LED is around 1 mm^2 (column 2, lines 26-30). This area is commensurate with the chip area itself, as shown in for example figure 1, where the light emitting area is identified as the upper area of the chip. It would have been obvious to make the light emitting device of the Japan 11-026647 reference of the same area as taught by Tamaoki et al, because the Tamaoki reference is describing typical prior art LEDs. Yamamoto et al. teaches sintered aluminum nitride as a substrate material for light-emitting diode devices

(column 16, lines 9-14). As taught in the abstract of this reference, this material has thermal conductivity greater than that required by claim 1. It would have been obvious to use the Yamamoto et al. material as substrate material for the device of the Japan 11-026647 reference, to obtain the desirable properties of such a substrate as taught by Yamamoto et al. Note that the Yamamoto substrate is 1.5 mm thick (column 23, line 19), which is also a good deal larger than 0.3 times the 1mm chip length of the Tamaoki light emitting chip. The substrate and chip dimensions of the prior art devices of Tamaoki et al. and Yamamoto et al. are thus comparable to those shown in the figure of the Japan 11-026647 reference.

With respect to claim 2, the chip of the Japan reference is in a cavity, and the upper electrode is on the top surface. Metal for the upper electrode would have been obvious because this is the usual electrode material, used for its high conductivity. With respect to claim 3, the device of the Japanese reference has a terminal plate (2b at the bottom of the substrate) that supplies power to the light emitting element through a connection member formed of a vertical conductor (on the sidewall of the substrate) and a horizontal conductor (on the top of the substrate), which is spaced apart from the cavity.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to S. Crane, whose telephone number is (571) 272-1652.

The supervisor for Art Unit 2811, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sara W Crane

Sara W. Crane
Primary Examiner
Art Unit 2811